Code: 20IT3402

II B.Tech - II Semester – Regular / Supplementary Examinations MAY - 2024

COMPUTER ORGANIZATION (INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.

2. All parts of Question must be answered in one place.

| | | | BL | СО | Max. Marks | | |
|---------|----|--|----|-----|---------------|--|--|
| | | UNIT-I | | | <u> </u> | | |
| 1 | a) | Define Register transfer language, List and | L1 | CO1 | 7 M | | |
| | | explain arithmetic micro operations. | | | | | |
| | b) | Write RTL statements for the following | L2 | CO1 | 7 M | | |
| | | operations: | | | | | |
| | | i) BUN ii) BSA iii) ISZ | | | | | |
| OR | | | | | | | |
| 2 | a) | List some data transfer instructions and | L1 | CO1 | 7 M | | |
| | | explain with an example. | | | | | |
| | b) | Explain the use of multiplexer to transfer | L2 | CO1 | 7 M | | |
| | | information from two source registers to one | | | | | |
| | | destination register with a neat diagram. | | | | | |
| | | | | | | | |
| UNIT-II | | | | | | | |
| 3 | a) | Discuss about Memory Reference | L1 | CO1 | 7 M | | |
| | | Instructions in detail. | | | | | |
| | | | | | | | |

| | b) | Describe the sequence of steps that takes | L2 | CO1 | 7 M |
|---|----|---|----|-----|-----|
| | | place during the instruction life cycle. | | | |
| | • | OR | | | |
| 4 | a) | Explain the interrupt cycle execution with | L2 | CO1 | 7 M |
| | | the help of a neat diagram. | | | |
| | b) | Illustrate the Input-Output Configuration | L3 | CO1 | 7 M |
| | | with all the input output instructions in | | | |
| | | detail. | | | |
| | | | | | |
| | | UNIT-III | | | |
| 5 | a) | Explain how $X = (A+B*C)/(A-B-C)$ is | L3 | CO2 | 7 M |
| | | evaluated in stack based computer. | | | |
| | b) | An Instruction is stored at location 300 with | L3 | CO2 | 7 M |
| | | its address field at location 301. The address | | | |
| | | field has the value 400. A processor register | | | |
| | | R1 contains the number 200. Evaluate the | | | |
| | | effective address if the addressing mode of | | | |
| | | the instruction is: | | | |
| | | i) Immediate | | | |
| | | ii) Direct | | | |
| | | iii) Register – indirect | | | |
| | | iv) Relative | | | |
| | | v) Index with R1 as the index register. | | | |
| | | OR | | | |
| 6 | a) | Illustrate the various categories of the set of | L1 | CO2 | 7 M |
| | | instructions associated with a computer. | | | |
| | b) | List out and explain the various typical | L2 | CO2 | 7 M |
| | | program control instructions. | | | |
| | | | | | |
| | | | | | |

| | | UNIT-IV | | | | | | |
|----|----|---|----|-----|-------|--|--|--|
| 7 | a) | Give means to identify on whether or not an overflow has occurred in 2's complement addition or subtraction operations. Describe | L3 | CO3 | 7 M | | | |
| | | with an example for each possible situation | | | | | | |
| | b) | by assuming 4- bit registers. Explain Booth's multiplication Algorithm. | L2 | CO3 | 7 M | | | |
| | U) | OR | | CO3 | / IVI | | | |
| 8 | a) | Explain various cache memory mapping techniques. | L2 | CO3 | 7 M | | | |
| | b) | Describe the following i) Need for cache memory. ii) Principle of locality of reference. | L1 | CO3 | 7 M | | | |
| | | UNIT-V | | | | | | |
| 9 | a) | Give a detailed comparison between Programmed I/O and Interrupt initiated I/O. | L4 | CO4 | 7 M | | | |
| | b) | Explain daisy-chain priority method. | L2 | CO4 | 7 M | | | |
| | OR | | | | | | | |
| 10 | a) | What are the four ways by which we can achieve parallelism according to Flynn's classification? | L1 | CO4 | 7 M | | | |
| | b) | Perform the arithmetic operation (A_i+B_i) + (C_i+D_i) with a stream of number. Specify a pipeline configuration to carry out the task. List the contents of all registers in the pipeline for i=1 through 6. | L3 | CO4 | 7 M | | | |